**Low Power And Area Efficient Wallace Tree Multiplier Using Carry Select Adder With Binary To Excess-1 Converter**

**Abstract**

Multipliers are major blocks in the most of the digital and high performance systems such as Microprocessors, Signal processing Circuits, FIR filters etc. In the present scenario, Fast  
multipliers with less power consumption are leading with their performance. Wallace tree multiplier with carry select adder (CSLA) is one of the fastest multiplier but utilizes more area. To improve the performance of this multiplier, CSLA is replaced by binary excess-1 counter(BEC) which not only reduces the area at gate level but also reduces power consumption. Area and power calculations for the Wallace tree multiplier using CSLA with BEC are giving good results compared to regular Wallace tree multiplier

**Tools:**

* Modelsim 6.4b
* Xilinx ISE 10.1

**Languages:**

* VHDL/Verilog HDL